TSMC01-1020

A NEW APPROACH TO PREVENT SPACER UNDERCUT BY LOW TEMPERATURE NITRIDATION

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method to prevent gate spacer undercut in the creation of gate electrode structures.

(2) Description of the Prior Art

The art of creating Complementary Metal Oxide Silicon (CMOS) devices is well known in semiconductor technology. Fig. 1 shows a cross section of a conventional CMOS device, the creation of this device will be briefly highlighted using the device elements that are highlighted in Fig. 1. The process of creating a CMOS device starts by providing a semiconductor substrate 10. Insulation regions 12, that bound the active region in the surface of substrate 10, isolate the active region in the surface of substrate 10 and may be created using Oxide (FOX) isolation or Shallow Trench Isolation (STI). A thin layer 16 of gate oxide is grown over the surface of the substrate 10 in the active device region. To create the gate structure, a layer 14 of

polysilicon is grown over the thin layer 16 of gate oxide. The polysilicon layer 14 is masked and the exposed polysilicon and the thin layer of oxide are etched to create the polysilicon gate 14 that is separated from the substrate 10 by the remaining thin layer 16 of oxide. The doping of the source/drain regions starts with creating the lightly N^+ doped diffusion (LDD) regions 32/34. The sidewall spacers 22 for the gate structure are formed after which the source (18) and drain (20) regions doping is completed by doping these source/drain regions 18/20 to the desired level of conductivity using an impurity implantation.

Low resistivity contact points 24 (to the source 18), 26 (to the drain 20) and 28 (to the electrode gate 14) are then formed by first depositing a layer of titanium or cobalt with TiN over the surface of the source/drain regions and the top surface of the gate electrode. This titanium or cobalt is annealed causing the deposited titanium or cobalt to react with the underlying silicon of the source/gain regions and the doped surface of the gate electrode. This anneal forms layers of titanium silicide or cobalt silicide 24/26 on the surfaces of the source/drain regions and layer 28 on the top surface of the gate electrode. Cobalt with TiN are used to form cobalt salicide in which the TiN serves as a barrier layer.

Metal contacts with the source (40) and drain (42) regions and the gate electrode (44) are formed as a final step. A layer 30 of dielectric, such as silicon oxide, is blanket deposited over the surface of the created structure. This layer of dielectric is patterned and etched to create contact openings 36/37 over the source/drain regions and opening 38 over the top surface of the gate electrode. A metallization layer is deposited over the patterned layer 30 of dielectric, establishing the electrical contacts 40/42 with the source/drain regions and 44 with the top surface of the gate electrode.

The conventional methods that are employed to create CMOS devices address such concerns as the thickness and uniformity of the layer of gate oxide, a shallow junction depths required for the device impurity implantations, the impurity content of the layer of gate dielectric, the dielectric constant of the materials for the gate dielectric, prevention of the migration of impurity implantations (such as boron, implanted into a layer of polysilicon to create the conductivity of the body of the gate electrode) into the channel region of the underlying substrate, causing leakage current of the gate electrode to the substrate, device switching speed and the like.

The invention addresses concerns of damage that is caused to the layer of gate spacer oxide. The layer of gate spacer oxide (also referred to as liner oxide) underlies the gate spacers and is interposed between the body of the gate electrode and the gate spacers, overlying the sidewalls of the body of the gate electrode. An overetch of the layer of gate spacer oxide causes the gate spacer oxide to be partially removed from below the gate spacer, creating an undercut below the gate spacer. Methods are provided by the invention to prevent this undercut.

US 6,200,868 B1 (Mase et al.) shows a nitridation process to prevent gate spacer undercut.

US 6,187,676 (Kim et al.) shows a nitridation process to cover an undercut.

US 6,144,071 (Gardner) shows a related method.

SUMMARY OF THE INVENTION

It is the primary objective of the invention to reduce undercut in the layer of gate spacer oxide of a gate electrode.

Another objective of the invention is to improve isolation of the gate electrode.

Yet another objective of the invention is to prevent the accumulation of semiconductor materials or foreign particles in openings created under the gate spacers of a gate electrode.

In accordance with the objectives of the invention a new method is provided for the removal of liner oxide from the surface of a gate electrode during the creation of the gate electrode. A layer of gate oxide is formed over the surface of a substrate, a layer of gate electrode such as polyimide is deposited over the layer of gate oxide. The gate electrode and the layer of gate oxide are patterned. A layer of liner oxide is deposited, gate spacers are formed over the liner oxide, exposing surfaces of the liner oxide. The created structure is nitrided by a plasma stream containing N_2/H_2, reducing the etch rate of the exposed liner oxide. The liner oxide is then removed by applying a wet etch, contact regions to the gate electrode are salicided.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a cross section of a conventional gate electrode.

Figs. 2 through 4 show the occurrence of an undercut in a layer of liner oxide that is created between a gate spacer and the body of a gate electrode.

Figs. 5 through 7 show a first sequence of creating salicided contact regions to a gate electrode and the effect of an undercut in the layer of liner oxide thereon.

Figs. 8 through 10 show a second sequence of creating salicided contact regions to a gate electrode and the effect of an undercut in the layer of liner oxide thereon.

Figs. 11 through 15 show the processing of the invention, specifically:

Fig. 11 shows a cross section of a gate electrode, a layer of liner oxide has been deposited, gate spacers of reduced height have been created over sidewalls of the gate electrode.

Fig. 12 shows the gate electrode during the application of an N_2/H_2 plasma to the exposed surfaces.

Fig. 13 shows a cross section of a protective layer that has been formed over the exposed surfaces of the structure by the N_2/H_2 plasma.

Fig. 14 shows a cross section after removal of the liner oxide from the exposed surfaces.

Fig. 15 shows a cross section after salicided contact surfaces have been formed for the gate electrode.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The creation of a conventional CMOS device has previously been highlighted using the cross section of Fig. 1. An alternate method of creation a gate electrode is shown in the cross section of Fig. 2. Specifically shown in the cross section of Fig. 2 are:

- 51, two STI regions defined in the surface of the substrate 10, these STI region 51 electrically isolates the gate electrode 53 from the other semiconductor devices (not shown) that have been created over the surface of substrate 10
- 53, a CMOS device created over the surface of substrate 10
- 14, a layer of gate material of the gate electrode of the CMOS device 53, typically comprising polysilicon

- 16, a layer of pad or gate oxide that has been formed over the surface of substrate 10
- 50, a layer of liner oxide, deposited over the surface of the substrate, including the surface of the gate electrode 53
- 52, a layer of nitride, deposited over the surface of the layer 50 of liner oxide.

Typically, a blanket layer 16 of pad oxide can be formed over the surface of a silicon substrate through a thermal oxidation method at a temperature of about 900 degrees C. for a time period of about 10 to 20 minutes. A layer 16 of pad oxide is typically formed to a thickness of between about 50 and 150 Angstrom.

For the creation of a typical gate electrode, such as gate electrode 53 shown in cross section in Fig. 2, a layer 14 of polysilicon is deposited over the layer 16 of gate oxide and etched using photolithography followed by anisotropic poly etch. The etch to form the body 14 of the gate electrode 53 removes the layer of poly and the layer of gate oxide from above the surface of substrate 10 in accordance with the pattern of the gate electrode 53.

After layers 14 and 16 have been patterned and etched, a self-aligned LDD implantation (not shown, shown as implantations 32/34 in Fig. 1) is performed into the surface of the substrate 10.

Layer 50, Fig. 2, is an oxide liner, layer 52 is a layer of silicon nitride. Combined, the layers 50 and 52 form a passivation layer over the surface of the substrate 10 and the gate electrode 53. Passivation layers typically contain an oxide or nitride, they can also contain SiO_2 that is deposited by plasma at low temperatures, a SACVD oxide layer, a plasma enhanced nitride layer or a LPCVD oxide. Silicon nitride is used as a passivation layer due to its ability to provide an impermeable barrier to moisture and mobile impurities (e.g. sodium ions). Silicon nitride also forms a tough coating that protects an underlying integrated circuit against mechanical damage.

Layer 50 of liner oxide is native oxide or thermally grown oxide or CVD deposited oxide, to a thickness of between about 100 and 500 Angstrom, layer 52 of nitride is deposited next.

Layer 52 of silicon nitride is deposited over the surface of the liner oxide layer 50. The layer 52 of silicon nitride (Si_3N_4) can be deposited using LPCVD or PECVD procedures at a pressure between about 300 mTorr and 400 mTorr, at a temperature between about 600 and 800 degrees C., to a thickness of between about 2,000 and 3,000 Angstrom using NH_3 and SiH_4. The silicon nitride layer 52 can also be deposited using LPCVD or PECVD procedures using a reactant gas mixture such as dichlorosilane ($SiCl_2H_2$) and amonia (NH_3).

Gate spacers for gate electrodes are typically created using a variety of materials such as silicon oxide, BSG, PSG, other materials preferably of a dielectric nature and CVD oxide formed from a TEOS source.

Fig. 3 shows a cross section of the structure of Fig. 2 after the layer 52 of silicon nitride has been etched, stopping on the layer 50. Shown in Fig. 3 are spacers 52 of silicon nitride created on the sidewalls of the gate electrode 53. The preferred method of the invention for the etch of the layer 52 of silicon nitride is a dry etch such as applying an RIE etch using CHF_3 or SF_6-O_2 as an etchant.

After the gate spacers 52 have been created as shown in cross section in Fig. 3, the layer 50 of liner oxide must be removed from the surface of substrate 10 where the surface of this layer 50 is exposed. This process of removal can be performed by etching layer 50 (Fig. 3) using Ar/CF_4 as an etchant at a temperature of between about 120 and 160 degrees C. and a pressure of between about 0.30 and 0.40 Torr for a time of between about 33 and 39 seconds using a dry etch process. Silicon oxide layer 50 can also be etched via anisotropic RIE of the silicon oxide layer 50, using CHF_3 or CF_4-O_2-He as an etchant.

The results of this latter etch are shown in cross section in Fig. 4. Specifically highlighted in the cross section of Fig. 4 are regions 54 which are the regions where the etched layer 50 of liner oxide is attacked by the etch to the point where the etch proceeds underneath the gate spacers 52, resulting in loss of liner oxide in the interface between the gate spacers 52 and the body 14 of the gate electrode 53 and in the interface between the gate spacer 52 and the substrate 10. Due to the loss of liner oxide in these regions 54, device isolation and device performance is negatively affected, this loss of liner oxide must therefore be avoided. The invention provides a method that results in avoiding the loss of liner oxide in regions 54 of the created gate electrode.

Various processing steps are further conventionally performed to improve gate spacer performance, these processing steps will be briefly highlighted in the following Figs. 5 through 10.

Fig. 5 shows the now familiar cross section of a gate electrode, spacers 52 of silicon nitride have been formed over the sidewalls of the gate electrode with a layer 50 of liner oxide being interposed between the silicon nitride gate spacers 52 and the body 14 of the gate electrode. The etch of layer 52 of silicon nitride and the layer 50 of liner oxide over the surface of the gate electrode, Fig. 5, has resulted in an accumulation of the liner oxide 50 in a profile that is highlighted with the boundary lines 55. This liner oxide must as yet be removed from the surface in addition to removing the liner oxide 50 where this liner oxide overlies the surface of substrate 10.

This removal of liner oxide 50 can be performed by applying a wet etch process to the exposed surface of the structure, resulting in a cross section that is shown in Fig. 6. The liner oxide 50 has been removed from the surface of the created gate spacers 52 of silicon nitride but, as a negative consequence of this removal, an undercut 57 (four such undercuts are highlighted in the cross section of Fig. 6) into the liner oxide 50 and

located underneath the gate spacers 52 is also created. The undercut 57 has been measured to penetrate about 300 Angstrom underneath the etched layer 52 of silicon nitride gate spacer, the height of the gate spacers 52 is about equal to the height of the body 14 of the gate electrode measured in a direction that is perpendicular to the surface of substrate 10. This measure of 300 Angstrom gives an approximate indication of how far the next to be created layer of salicidation material will penetrate underneath the gate spacers 52 in a downward direction along the sidewalls of the body 14 of the gate electrode.

Saliciding the contact surfaces of the gate electrode, using for instance cobalt as a salicidation material, results in creating the salicided surfaces 59, Fig. 7, to the source/drain surfaces of the gate electrode and salicided surface 60 to the body 14 of the gate electrode. It is clear from the cross section that is shown in Fig. 7 that the salicidation material, in the cited example being $CoSi_x$, penetrates underneath the gate spacers 52.

To further improve device performance, by decreasing sheet resistance of the salicided region 60 of Fig. 7, the salicided layer can be increased. This is shown in the cross sections of Figs. 7 through 10.

The cross section of Fig. 8 shows how the height of the silicon nitride gate spacers 52 is further reduced with respect to the height of layer 14 of the body of the gate electrode, liner oxide 50 is now accumulated bounded by line 55' of the cross section of Fig. 8. The difference in height between the gate spacers 52 and the top surface of the body 14 of the gate electrode has been measured as being about 600 Angstrom, this difference has to be compared with the previously cited difference in height (Fig. 6) of about 300 Angstrom in order to get an appreciation for the potential increase in the size of the salicided layer 60 and the therewith associated reduction in sheet resistance of this salicided layer.

The liner oxide 50, Fig. 8, is next removed, again applying a wet process to the surface of the structure, resulting in the cross section that is shown in Fig. 9. An undercut 57' is again experienced, now creating the salicided contact surfaces 59' and 60' of the gate electrode as shown in the cross section of Fig. 10.

It is clear in comparing the cross section of Fig. 7, where a first salicided layer 60 over the top surface of the gate electrode is shown, with the cross section of Fig. 10, where a second salicided layer 60' over the top surface of the gate

electrode is shown, that the second salicided layer 60' is considerably larger than the first salicided layer 60. From this it can be concluded that the contact resistance to the top surface of the gate electrode that is shown in cross section in Fig. 10 is considerably lower than the contact resistance to the top surface of the gate electrode that is shown in cross section in Fig. 7.

While therefore the procedure that is highlighted with the cross sections of Figs. 8 through 10 results in improved device performance, this improved device performance results in having created salicided layers that are now located in extreme proximity to the layer 16 of gate oxide of the gate electrode. The invention provides a method that negates this incurred disadvantage. This is explained in detail in the following Figs. 11 through 15.

Fig. 11 will be recognized as being the same cross section as the cross section that has previously been discussed under Fig. 8 and does therefore not need any further discussion at this time. Fig. 11 is shown at this time since it is the structure of the gate electrode that must first be formed before the unique processing steps of the invention are performed.

Layer 16 of gate oxide is preferably created to a thickness between about 50 and 150 Angstrom, layer 14 of gate material preferably comprises polysilicon and is preferably deposited to a thickness between about 3,000 and 7,000 Angstrom, the layer of gate spacer material that is deposited for the formation of gate spacers 52 preferably comprises silicon nitride and is preferably deposited to a thickness between about 2,000 and 3,000 Angstrom, the layer 50 of liner oxide is preferably created to a thickness between about 100 and 500 Angstrom.

What must be emphasized in the cross structure that is shown in Fig. 11 is that the top surface of the liner oxide 50, where this liner oxide 50 is present over the sidewalls of the body 14 of the gate electrode and is interspersed between the gate spacers 52 and layer 14, is exposed in surface area 61. This is of importance since this offers the opportunity to specially treat this exposed surface 61 of the layer of liner oxide.

The special treatment of the exposed surface of the layer of gate oxide 50 is highlighted in the cross section of Fig. 12, where exposed surfaces of the structure that is shown in cross section in Fig. 11 are nitrided by being exposed to a down-stream N_2/H_2 plasma. This plasma exposure 62 results in significantly reducing the etch rate of the liner oxide, which for instance can

be TEOS. It has been experimentally confirmed that the N_2/H_2 plasma treatment, which is preferably a low temperature treatment performed at a temperature of about 250 degrees C., reduces the etch rate of the liner oxide by about 35 to 36%. If SiO_x is used as the material of choice for the oxide liner, the N_2/H_2 plasma treatment will isotropically nitridize the SiO_x to SiO_xN_y, which results in reducing the rate at which the liner oxide will be removed during subsequent processing.

The N_2/H_2 plasma treatment will therefore effectively create a layer 64, Fig. 13, of for instance SiO_xN_y, over the exposed surfaces of the structure that is shown in cross section in Fig. 12. This is of special significance for the regions that have been highlighted as regions 65 in the cross section of Fig. 13, since these are the regions where the problem of undercut has previously been experienced.

The exposed surfaces of the cross section that is shown in Fig. 13 are now again wet etched, with the created layer 64 acting as a protective layer against the typically experienced undercut. Small spacer protection is in this manner provided in regions 65, Fig. 65, eliminating the undercut phenomenon. The cross section of the structure, after completion of the exposure to wet etch of the structure of Fig. 13, is shown in Fig. 14.

The structure of Fig. 14 is now ready for the creation of salicided contact surfaces over the gate electrode. The results of this salicidation process are shown in the cross section of Fig. 15. Region 60" has been highlighted as the salicided contact to the top of the gate electrode while regions 59" have been highlighted as the salicided surfaces of the source/drain regions of the gate electrode.

Since, for reasons cited above, the salicided surfaces cannot enter underneath the gate spacers 52, while at the same time maintaining a relatively large salicided region 60", the advantage of improved gate performance (by means of reduced sheet resistance) has been gained without incurring potential problems of electrical discharge from the created salicided surfaces, most notably the salicided top surface of the gate electrode, to the layer of gate oxide of the gate electrode, resulting in damage to the layer of gate oxide of the gate electrode.

Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. It is therefore intended to

include within the invention all such variations and modifications which fall within the scope of the appended claims and equivalents thereof.